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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>10 March 2009</u>.
2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-28* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☐ All   b)☐ Some * c)☐ None of:
      1.☐ Certified copies of the priority documents have been received.
      2.☐ Certified copies of the priority documents have been received in Application No. _____.
      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.
4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments, filed 3/10/2009, with respect to the rejection(s) of claim(s) 1-28

under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has

been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in

view of Dawson et al. (US20050028225), Machida, and other references of record.

Claim Rejections - 35 USC § 112

2.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the
> subject matter which the applicant regards as his invention.

3.   Claim 26 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for

failing to particularly point out and distinctly claim the subject matter which applicant regards as

the invention.

        Claim 26 recites, "wherein the video data". Claim 26 is vague because it is unclear if "the

video data" of claim 26 is intended to refer back to the video data of claim 19, line 1, the video

data of claim 19, line 4, the video data of claim 19, line 8, or the video data of claim 19, line 14.

        Appropriate correction is required.

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

5.   Claims 1, 4-5, 7-8, 11-12, 19, 22 and 26 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Machida (of record) in view of Dawson et al. (US20050028225, hereinafter

Dawson).

        Regarding claims 1, 7 and 19, Machida discloses an apparatus for display of video data

(image generation apparatus 100, see Fig. 3), the apparatus comprising:

        a switch network (image selection means 101, see Fig. 3) including an output (see Fig. 3)

and an input (see Fig. 3), and

        a plurality of video processing pipelines (image processing means 102, see Fig. 3), each

video processing pipeline including an input coupled to the switch network output (see Fig. 3),

wherein the switch network is configured to connect any of the switch inputs to any of the video

processing pipeline inputs (see Fig. 3).

        Machida does not specifically disclose a plurality of video sources,

        a plurality of video channels configured to be coupled to different video sources,

a plurality of video decoders coupled to the plurality of video channels, each video decoder coupled to a different one of the plurality of video channels and comprising:

an output, and

an input coupled to one or more video channels, to receive video data from the one or more video channels, and to decode the received video data, or

a switch network including an output and an input coupled to the video decoder outputs.

In an analogous art, Dawson discloses a plurality of video sources (analog video sources 34, see Fig. 1A),

a plurality of video channels configured to be coupled to different video sources (see [0027], lines 1-3 and Fig. 1A),

a plurality of video decoders (analog video decoders 22, see Fig. 1A) coupled to the plurality of video channels (see Fig. 1A), each video decoder coupled to a different one of the plurality of video channels (see Fig. 1A) and comprising:

an output (see Fig. 1A), and

an input coupled to one or more video channels (see Fig. 1A), to receive video data from the one or more video channels (see [0027], lines 1-3 and Fig. 1A), and to decode the received video data (see Fig. 1A), and

a switch network (analog source router MUX 24, see Fig. 1A, which corresponds to Machida's image selection means 101) including an output (see Fig. 1A) and an input coupled to the video decoder outputs (see Fig. 1A; the video decoder outputs of Dawson correspond to the image inputs/switch inputs of Machida, see Machida, Fig. 3).

It would have been obvious for a person having ordinary skill in the art at the time of the

invention to modify Machida's system to include the limitations as taught by Dawson for the

advantage of providing a variety of media content from various sources to be displayed while

preserving the transport portion of system resources across stream source selections.

Regarding claim 4, Machida in view of Dawson discloses a plurality of video processing

pipelines (image processing means 102, see Machida, Fig. 3) configured to process decoded

video data (the decoded video data of Dawson, see Fig. 1A, corresponds to the image inputs of

Machida, as the analog source router mux 24 of Dawson corresponds to the image selection

means 101 of Machida, see Machida, Fig. 3) of a plurality of video sources (see Dawson, Fig.

1A) received from a plurality of video decoders (see Dawson, Fig. 1A).

Regarding claims 5, 8 and 22, Machida in view of Dawson discloses a greater number of

video decoders than video processing pipelines (Machida discloses that the images selected to be

output may be less than the images input, and therefore the plurality of video processing means

are respective to the images selected to be output, see Machida, col 5, lines 28-41 and Fig. 3;

since the image inputs of Machida correspond to the video decoder outputs of Dawson, Machida

in view of Dawson reasonably teaches a greater number of video decoders than video processing

pipelines) and wherein the apparatus further comprises a display/control logic (screen control

means 106, see Machida, Fig. 3) configured to control a process order of the video data from the

plurality of video sources (see Machida, col 5, lines 17-19).

Regarding claim 11, Machida in view of Dawson discloses decoding, with a plurality of

video decoders, a portion of video data comprises decoding, with the plurality of video decoders,

a frame in the video data (since an entire video signal is decoded, a frame of video is therefore

decoded, see Dawson, Fig. 1A).

Regarding claim 12, Machida in view of Dawson discloses decoding, with a plurality of

video decoders, a portion of video data comprises decoding, with the plurality of video decoders,

a field of a frame in the video data (since an entire video signal is decoded, a frame of video is

therefore decoded, and therefore a field of a frame is decoded, see Dawson, Fig. 1A).

Regarding claim 26, Machida in view of Dawson discloses analog video data (see

Dawson, Fig. 1A).

6.   Claims 2-3 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Machida (of record) in view of Dawson (previously cited), as applied to claims above, and

further in view of Itoh (of record).

Regarding claims 2 and 20, Machida in view of Dawson discloses an image size/location

logic (image selection means 101/adapted image synthesization means 105/screen control means

106, see Machida, Fig. 3) coupled to each video processing pipeline output (see Machida, Fig.

3), the image size/location logic configured to receive a signal indicating designated size of a

display window (display window size must be designated since the sizes of the images are

designated in proportion to the screen size, see Machida, col 5, lines 17-27), the image

size/location logic further configured to determine a location in the display window (see

Machida, col 5, lines 56-58 and col 6, line 1) and a size of a part of the display window for

display for the video data (see Machida, col 5, lines 17-23) for each of the plurality of video sources (see Dawson, Fig. 1A) including video data for display (see Machida, col 5, lines 17-23).

Machida in view of Dawson does not specifically disclose an indication of which of a plurality of video sources includes video data for display in a display window.

In an analogous art, Itoh discloses an indication of which of a plurality of video sources includes video data for display in a display window (see col 12, lines 53-60).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Dawson to include the limitations as disclosed by Itoh, for the advantage of conserving the processing resources of the system by only providing only the necessary processing for specific signals.

Regarding claims 3 and 21, Machida in view of Dawson, and further in view of Itoh discloses a plurality of scalers (image processing means 102, see Machida, Fig. 3) coupled to a plurality of video decoders (see Dawson, Fig. 1A) and a plurality of video processing pipelines (see Machida, Fig. 3), wherein the plurality of scalers are each configured to scale decoded video data from the plurality of video sources (see Machida, col 5, lines 36-41 and Fig. 3) based on the determined size of the part of the display window (see Machida, col 5, lines 17-23).

7.   Claims 6 and 9-10 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Dawson (previously cited), as applied to claims 1 and 7 above, and further in view of Miyazaki (of record).

Regarding claims 6 and 27, Machida in view of Dawson discloses a plurality of video processing pipelines, a plurality of video sources and processed decoded data, but does not specifically discloses a memory device, or a write multiplexer coupled to the memory device, the write multiplexer configured to receive data and store the data into the memory device.

In an analogous art, Miyazaki discloses a memory device (VRAM 18A, see Fig. 1), and a write multiplexer (mux 12, see Fig. 1) coupled to the memory device, the write multiplexer configured to receive data and store the data into the memory device (see Fig. 1).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Dawson to include the limitations as disclosed by Miyazaki for the advantage of sequentially storing I-frames as they are decoded, thereby reducing the latency of switching signals.

Regarding claim 9, Machida in view of Dawson, and further in view of Miyazaki discloses storing a processed decoded portion of video data into a portion of a video buffer that is not updating the display (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

Regarding claim 10, Machida in view of Dawson, and further in view of Miyazaki discloses switching the portion of the video buffer that is not updating the display with a portion of the video buffer that is updating the display (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14), upon determining (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14) that the plurality of video processing pipelines (see Machida, Fig. 3) has completed processing the decoded portion of the video data (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

Regarding claim 28, Machida in view of Dawson, and further in view of Miyazaki discloses a clock multiplier network (see Miyazaki, col 13, line 35), the clock multiplier network controlling a rate of operation of the write multiplexer (see Miyazaki, col 13, lines 35-37).

8.   Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Dawson (previously cited), as applied to claim 7 above, and further in view of Reitmeier (of record).

Regarding claim 13, Machida in view of Dawson discloses decoding, with a plurality of video decoders, a portion of video data comprises decoding, with the plurality of video decoders, but does not specifically disclose decoding a scaled field of a frame in the video data.

In an analogous art, Reitmeier discloses decoding a scaled field of a frame in the video data (see Reitmeier, col 5, lines 62-65 and col 6, lines 5-7).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Dawson to include the limitations as disclosed by Reitmeier for the advantage of conserving memory resources.

9.   Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Dawson (previously cited), as applied to claims 1 and 7 above, and further in view of Reitmeier (of record) and Miyazaki (of record).

Regarding claim 14, Machida discloses a method for displaying video data, comprising:

inputting an image into a first video processing pipeline (image processing means 102, see Fig. 3) via a non-blocking switch network (image selection means 101, see Fig. 3);

inputting a second image into a second video processing pipeline (image processing means 102, see Fig. 3) via the non-blocking switch network (image selection means 101, see Fig. 3);

processing, by the first video processing pipeline the first image (see Fig. 3);

processing, by the second video processing pipeline the second image (see Fig. 3).

Machida does not specifically disclose receiving a first video data from a first video source at a first video decoder via a first video channel;

receiving a second video data from a second video source at a second video decoder via a second video channel;

decoding, via the first video decoder, a first frame of the first video data;

decoding, via the second video decoder, a second frame of the second video data;

inputting the first decoded frame into an image into a first video processing pipeline (image processing means 102, see Fig. 3) via a non-blocking switch network (image selection means 101, see Fig. 3);

inputting the second decoded frame into a second image into a second video processing pipeline (image processing means 102, see Fig. 3) via the non-blocking switch network (image selection means 101, see Fig. 3)

processing, by the first video processing pipeline the first image (see Fig. 3) decoded frame;

processing, by the second video processing pipeline the second image (see Fig. 3) decoded frame;

transmitting the processed first decoded frame into a first portion of a video buffer for updating the display with the processed first decoded frame; and

storing the second processed decoded frame into a second portion of the video buffer that is not updating the display.

In an analogous art, Dawson discloses receiving a first video data from a first video source at a first video decoder via a first video channel (see Fig. 1A);

receiving a second video data from a second video source at a second video decoder via a second video channel (see Fig. 1A);

decoding, via the first video decoder, a first frame of the first video data (since an entire video signal is decoded, a frame of video is therefore decoded, see Dawson, Fig. 1A);

decoding, via the second video decoder, a second frame of the second video data (since an entire video signal is decoded, a frame of video is therefore decoded, see Dawson, Fig. 1A);

inputting the first decoded frame (since an entire video signal is decoded, a frame of video is therefore decoded, see Dawson, Fig. 1A, the decoded video signals/frames of Dawson corresponding to the image inputs of Machida, see Machida, Fig. 3); and

inputting the second decoded frame (since an entire video signal is decoded, a frame of video is therefore decoded, see Dawson, Fig. 1A, the decoded video signals/frames of Dawson corresponding to the image inputs of Machida, see Machida, Fig. 3).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify Machida's system to include the limitations as taught by Dawson for the same advantage as stated above regarding claim 1.

Machida in view of Dawson does not specifically disclose transmitting the frame into a first portion of a video buffer for updating the display with the processed first decoded frame; and

storing the second frame into a second portion of the video buffer that is not updating the display.

In an analogous art, Reitmeier discloses transmitting a first frame to a video buffer of a video buffer for updating the display with the processed first decoded frame (see Reitmeier, Fig. 1 and col 3, lines 66-67 and col 4, lines 63-65).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Dawson to include the limitations as disclosed by Reitmeier for the advantage of providing a more efficient system for rapidly acquiring channels.

Machida in view of Dawson and Reitmeier does not specifically disclose transmitting a first frame into a first portion of a video buffer, and

storing the second processed decoded frame into a second portion of a video buffer that is not updating the display.

In an analogous art, Miyazaki discloses transmitting a first frame into a first portion of a video buffer (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14), and

storing the second processed decoded frame into a second portion of a video buffer that is not updating the display (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Dawson and Reitmeier to include the limitations as disclosed by Miyazaki for the advantage of reducing the latency of acquiring channels.

10.   Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Dawson (previously cited), Reitmeier (of record) and Miyazaki (of record), as applied to claim 14 above, and further in view of Miura (of record).

Regarding claim 15, Machida in view of Dawson, Reitmeier and Miyazaki discloses processing, by a first video processing pipeline, a decoded first frame, but does not specifically disclose determining whether a first video source coupled to the first video processing pipeline is in a failed state.

In an analogous art, Miura discloses determining whether a first video source coupled to the first video processing pipeline is in a failed state (see col 18, lines 56-63 and col 19, lines 1-9).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Dawson, Reitmeier and Miyazaki to include the limitations as disclosed by Miura for the advantage of eliminating unstable conditions of the system, and thereby improving the efficiency of the system.

Regarding claim 16, Machida in view of Dawson, Reitmeier and Miyazaki, and further in view of Miura discloses processing, by a first video processing pipelines, a first decoded frame comprising outputting a blacked out frame for a first video source upon determining that the first video source is in a failed state (see Miura, col 20, lines 49-54).

Regarding claim 17, Machida in view of Dawson, Reitmeier and Miyazaki, and further in view of Miura discloses switching a configuration of a second portion of a video buffer that is not updating a display with a part of a video buffer that is updating the display, upon determining that the first and second video processing pipelines have completed processing the first and second decoded frames (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

Regarding claim 18, Machida in view of Dawson, Reitmeier and Miyazaki, and further in view of Miura discloses scaling first and second decoded frames (see Reitmeier, col 5, lines 62-65 and col 6, lines 5-7) based on image size and the number of video sources (the number of video sources that are actually to be displayed, see Machida, col 5, lines 32-48).

11.   Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (of record) in view of Dawson (previously cited), as applied to claim 19 above, and further in view of Miura (of record).

Regarding claim 23, Machida in view of Dawson discloses a video processing pipeline, but does not specifically disclose executing a video fail operation if one of a plurality of video decoders does not lock onto video data from one of a plurality of video channels after a predetermined time.

In an analogous art, Miura discloses executing a video fail operation if one of a plurality of video decoders does not lock onto video data from one of a plurality of video channels after a predetermined time (see col 18, lines 56-63 and col 19, lines 1-9).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Machida in view of Dawson to include the limitations as disclosed by Miura, for the advantage of eliminating unstable conditions of the system, and thereby improving the efficiency of the system.

Regarding claim 24, Machida in view of Dawson, and further in view of Miura discloses a video fail operation comprising an output of a blacked out frame overlaid with a descriptive text to indicate video failure for the plurality of video sources (see Miura, col 20, lines 49-54).

Regarding claim 25, Machida in view of Dawson, and further in view of Miura discloses a video fail operation comprising an output of a previous image for the one of the plurality of video channels overlaid with a descriptive text to indicate video failure (see Miura, col 20, lines 49-54 and col 36, lines 20-33).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHENEA P. SMITH whose telephone number is (571)272-9524. The examiner can normally be reached on Monday through Friday, 7:30 am - 5:00 pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (571) 272-7353. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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